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Where to Contact for Help
Customer support is available by mail, fax, email or phone. Before contacting Customer Support, we recommend you re-checking this manual for help.

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Chapter 1 Introduction

MOXA C101, a high speed single port sync/async board, is equipped with an HD64570 SCA and 256K dual-ported RAM. HD64570 SCA supports a wide variety of protocols including Async, Byte Sync, Bit Sync (HDLC, SDLC, X.25, etc.). The built-in 32 byte FIFO and Direct Memory Access (DMA) controller help otherwise to boost the communication speed. Data is received from (transmitted to) the large RAM by DMA to enhance higher performance with lower CPU load.

1.1 Features

- Powerful serial communication controller, HD64570-10
- Multi-protocols supported including Async, Byte Sync, Bit Sync
- Built-in DMA for fast data transmission
- Built-in 32 byte FIFO to receive/transmit data
- Large data buffer with 256K bytes Dual-ported RAM
- 16K memory window for the Dual-ported RAM
- Jumper selectable for transmitting (in or out) clock direction
- Communication interface (RS-232 or V.35): jumper selectable
- RS-232 sync communication rate up to 128Kbps
- V.35 sync communication rate up to 7Mbps
Support DOS/Windows environment

1.2 Specifications

- SCA: HD64570-10, 9.8304M clock
- RAM: 256K Dual-ported RAM with 16K memory window
- RAM Address: Switch selectable. 32 possible base addresses.
- IRQ: 2, 3, 4, 5, 7, 10, 11, 12 or 15 jumper selectable
- Interface: RS-232 or V.35 jumper selectable
- TxC direction: in or out jumper selectable
- Drivers: DOS, Windows 3.1
- API: DOS: C, Assembly; Windows: DLL

1.3 Applications

- High speed Sync/Async modem communication
- ISDN modem, T1 DSU/CSU communication
- Long distance, high speed communication
- Satellite communication
Chapter 2

2.1 Hardware Configuration
### a. Base Address

It is by way of switch1 (SW1) to set the memory mapping base address. Each C101 Super-Sync Board will occupy 16KB memory window.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>1</th>
<th>2</th>
<th>3</th>
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<td>OFF</td>
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<tr>
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<tr>
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<td>OFF</td>
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<tr>
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<tr>
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<table>
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<tr>
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<td>ON</td>
</tr>
<tr>
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</tr>
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<td>CDC000</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

**b. IRQ**

By means of the jumper JP1 to select the IRQ number for C101 Super-Sync Board. There are 9 possible IRQ numbers available on:

2, 3, 4, 5, 7, 10, 11, 12, 15

c. **Communication Interface**

C101 provides RS-232, V.35 communication interfaces as well. In this case, jumper JP3 is used to select the desired interface.
d. Clock Direction

Jumper JP2 is used to select the transmit in or out clock direction

2.2 Software Configuration

MOXA C101 Driver diskette consists of the following files/dir.:

\DOS \DOS\DRIVER    DOS driver and example directory
\DOS\DRIVER\c101s.lib DOS driver directory
\DOS\DRIVER\c101m.lib DOS driver library for small model
\DOS\DRIVER\c101.h   DOS driver library for medium model
\DOS\EXAMPLE        Driver declare file
\DOS\EXAMPLE\ex1.c   DOS driver example directory
\DOS\EXAMPLE\c101.cnf DOS driver example program

\WIN \WIN\DRIVER    Windows driver and example directory
\WIN\DRIVER\msa.dll  Windows driver directory
\WIN\DRIVER\msa.lib  Windows DLL driver
\WIN\DRIVER\c101.h   Windows library
\WIN\EXAMPLE        Driver declare file
\WIN\EXAMPLE\ex1.c   Windows example directory
\WIN\EXAMPLE\c101.cnf Windows driver example program

\UTIL \UTIL\c101diag Utility directory
\UTIL\c101diag         C101 diagnostic utility

a. For DOS users

DOS users need to link C101 library to their application program,
c101s.lib for small model

c101m.lib for other models

In addition, users have to specify the configuration of C101 board in c101.cnf and put it in the working directory. File c101.cnf will be read when the driver is initialized.

b. *For Windows 3.x users*

Windows users need to move msa.dll and c101.cnf to the same working directory. Try to use example configuration file, c101.cnf, to test first.
Chapter 3 Library Functions

1. **sio_init**

   Syntax: int sio_init(void);

   Description:
   Initialize SCA (Serial Communication Adapter), prepare IRQ, set up system
   variables, allocate system memory. Read c101.cnf file for I/O address, and
   IRQ selected, (Please read the c101.cnf for more information). This function
   must be invoked before any other function.

   Return: 0 OK
   -xx error configuration file, please see "c101.h"

2. **sio_reset**

   Syntax: int sio_reset (void);

   Description:
   Reset SCA to default setting specified in c101.cnf file.

   Return: 0 OK
3. **sio_release**

Syntax: void sio_release(void);

Description:
Release IRQ channel, free system memory.

Return: None

4. **sio_read**

Syntax: int sio_read (char far *buf, int len);

Description:
Read data from receive buffer. C101 has two receive buffers, one is on board RAM (totally 180K), and the other is determined by PktCnt in c101.cnf (totally PktCnt * PktSize).

buf: data buffer for reading received data
len: data buffer maximum length

Return: n received data frame length
-1 reserved buffer space insufficient for received data

5. **sio_write**

Syntax: int sio_write(char far *buf, int len);

Description:
Write data to transmit buffer. C101 has 64K transmit buffer on board.

buf: data pointer for writing to transmit buffer
len: data length for writing to transmit buffer

Return: n data be write to transmit buffer, must be len
0 no room for transmit buffer
-1 len = 0 or len too large

6. sio_flush

Syntax: int sio_flush (int mode);

Description:
Flush transmit and receive buffer
mode: 0: flush receive buffer
      1: flush transmit buffer
      2: flush both the receive and transmit buffer

Return: 0 OK

7. sio_isoverrun

Syntax: unsigned long sio_isoverrun(void);

Description:
Get overrun frame count, and reset the count to 0, the overrun frame happens only when receive buffer is full.

Return: n total overrun frame count

8. sio_isunderrun

Syntax: unsigned long sio_isunderrun(void);

Description:
Get underrun frame count, and reset the count to 0, the underrun frame only happens when SCA is too busy.
9. **sio_isbadframe**

Syntax: `unsigned long sio_isbadframe(void);`

Description:
Get bad frame count, and reset the count to 0. Bad frame includes bad CRC, or oversized large size frames.

Return: `n` total bad frame count

10. **sio_iframe**

Syntax: `int sio_iframe(void);`

Description:
Get received frame count in receive buffer

Return: `n` total received frame count

11. **sio_oframe**

Syntax: `int sio_oframe(void);`

Description:
Get transmit frame count in transmit buffer.

Return: `n` total transmit frame count
12. \textit{sio_iframefree}

Syntax: int \textit{sio_iframefree(void)};

Description:
Get free frame count in receive buffer.

Return: \textit{n} total receive buffer free frame count

13. \textit{sio_oframefree}

Syntax: int \textit{sio_oframefree(void)};

Description:
Get free frame count in transmit buffer.

Return: \textit{n} total transmit buffer free frame count
## Chapter 4 Pin Assignments

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<thead>
<tr>
<th>RS-232</th>
<th>DB25</th>
<th>Signal</th>
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</thead>
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</tr>
<tr>
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<td>3</td>
<td>RxD</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>RTS</td>
</tr>
<tr>
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<td>5</td>
<td>CTS</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>DSR</td>
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<td>7</td>
<td>7</td>
<td>GND</td>
</tr>
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<td>DTR</td>
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<td>8</td>
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<tr>
<td>24</td>
<td>24</td>
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</tr>
<tr>
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<td>15</td>
<td>TxC (Tx clock direction: in)</td>
</tr>
<tr>
<td>17</td>
<td>17</td>
<td>RxC (Rx clock direction: in)</td>
</tr>
<tr>
<td>PIN</td>
<td>SIGNAL</td>
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<td>TxC+ (Tx clock direction: out)</td>
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</tr>
<tr>
<td>7</td>
<td>GND</td>
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</tbody>
</table>
Moxa Super-Sync Board C101 Programming information

1. Refer to the Hitachi HD64570 documentation for further information.

2. The board utilizes memory map. There is 256K on board memory and 16K memory with PC interface, an 8-bit data path accessible to the memory and a 32-page, 8K memory window in addition. Otherwise the host PC can only see 2 pages (16K). The first 8K is usually to map the first page. Yet the second page must utilize Memory page register (address) to switch between each page.

   The dual-port memory address relative to HD64570 from 0 to 0x3FFFF.

   The base address for PC selected with DIP switch (SW 1) on board.
   (For further information, see Chapter 2 Configuration)

3. The windows 16K is described by the following base addresses:

   0000h – 1CFFh: first bank (always the first page for memory)
   2000h - 3FFFh: second bank (switch page with the page register)

   1D00h - 1DFFh: memory page register, write only.
   Same as write to each byte of the range memory,
   otherwise you may write down the value 00h - 1Fh 32 pages in total.
Example: Write value 2 on address 0x1D00. The second bank memory address is 0x4000 – 0x5FFF for HD64570
1E00h - 1EFFh: HD64570 interrupt acknowledge, read only.
Same as read each byte of the range memory
Example: Read value 0x30 from address 0x1E00. The value 0x30 interrupt vector is released by HD64570.

1E00h - 1EFFh: RS232/V35 DTR signal, write only (DTR control register)
Same as write to each byte of the range memory
the bit 0 used only, 0 for OFF, 1 for ON

1F00h - 1FFFh: HD64570 register set
Example 1: Read or write address 0x1F1A. It means to read or write HD64570 register IVR.
Example 2: Read or write address 0x1F1C. It means to read or write HD64570 register IMVR.

4. How to reset the HD64570 with software:
Reset the HD64570 after read the memory page register and latch this read until next write to the memory page register.

5. Power on the DRAM is disabled until first write to DTR control register

6. The Tx clock directory is selected on the JP2.

7. The interface RS232 or V.35 is selected on the JP3.

8. The IRQ is selected on the JP1.

9. C101 utilizes only the HD64570 channel 0. RTS control must on the other hand utilize channel 1 to control the RTS pin signal. The interrupt is functioned on the mode of Single acknowledge however.

10. HD64570 uses CPU mode 0 on C101 board.